# GR8BUS pinout

## SLOT1

| | | B | | A | | |
|---|---|---|---|---|---|---|
| Ground (0V) | Power | GND | 1 | WAIT% | Input | Bus Wait Signal, Open Collector |
| Reset Signal | Output | RESET | 2 | D7 | I/O | Bus Data, bit 7 (MSB) |
| +5V | Power | +5V | 3 | D6 | I/O | Bus Data, bit 6 |
| Bus Interrupt Request, Open Collector | Input | INT% | 4 | D5 | I/O | Bus Data, bit 5 |
| +3.3V | Power | +3V3 | 5 | D4 | I/O | Bus Data, bit 4 |
| Slot Select, identified by slot number | Output | SLTx | 6 | D3 | I/O | Bus Data, bit 3 |
| -12V | Power | -12V | 7 | D2 | I/O | Bus Data, bit 2 |
| Reserved | | KANJI | 8 | D1 | I/O | Bus Data, bit 1 |
| +12V | Power | +12V | 9 | D0 | I/O | Bus Data, bit 0 (LSB) |
| Ground (0V) | Power | GND | 10 | CPUWAIT | Output | CPU Wait Signal (for CPU Board) |
| Bus Write | I/O | WR | 11 | CPUINT | Output | CPU Interrupt Signal (for CPU Board) |
| Bus Read | I/O | RD | 12 | BUSRQ | I/O | Bus Request (Device to CPU) |
| Bus Memory Request | I/O | MREQ | 13 | BUSACK | I/O | CPU Bus Request Acknowledge (CPU to Device) |
| Bus I/O Request | I/O | IORQ | 14 | SLDN% | Input | Variable Slow-Down signal, Open Collector |
| Bus M1 Cycle | I/O | M1 | 15 | NC | | Reserved |
| ROM Chip Select 4000-7FFF | Output | CS1 | 16 | A15 | I/O | Bus Address, bit 15 (MSB) |
| ROM Chip Select 8000-BFFF | Output | CS2 | 17 | A14 | I/O | Bus Address, bit 14 |
| ROM Chip Select 4000-BFFF | Output | CS12 | 18 | A13 | I/O | Bus Address, bit 13 |
| Memory Refresh | I/O | RFSH | 19 | A12 | I/O | Bus Address, bit 12 |
| System Clock | I/O | CLOCK | 20 | A11 | I/O | Bus Address, bit 11 |
| Slot 0.1 Select Signal | Output | SLT01 | 21 | A10 | I/O | Bus Address, bit 10 |
| Slot 0.2 Select Signal | Output | SLT02 | 22 | A9 | I/O | Bus Address, bit 9 |
| Slot 0.3 Select Signal | Output | SLT03 | 23 | A8 | I/O | Bus Address, bit 8 |
| Slot 3.0 Select Signal | Output | SLT30 | 24 | A7 | I/O | Bus Address, bit 7 |
| Slot 3.1 Select Signal | Output | SLT31 | 25 | A6 | I/O | Bus Address, bit 6 |
| Slot 3.2 Select Signal | Output | SLT32 | 26 | A5 | I/O | Bus Address, bit 5 |
| Slot 3.3 Select Signal | Output | SLT33 | 27 | A4 | I/O | Bus Address, bit 4 |
| Non-Maskable Interrupt, Open Collector | I/O | NMI% | 28 | A3 | I/O | Bus Address, bit 3 |
| +5V | Power | +5V | 29 | A2 | I/O | Bus Address, bit 2 |
| VDP Clock, 21.47727 MHz typical, CMOS | I/O | VDPCLK | 30 | A1 | I/O | Bus Address, bit 1 |
| Ground (0V) | Power | GND | 31 | A0 | I/O | Bus Address, bit 0 (LSB) |

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